

Xenergetic's GF 22 Compiler



Compiler Features	Compiler Options	Supported BE/FE Models
<ul style="list-style-type: none"> • Single rail design • Foundry bitcell based • Four metal layers • Peri Body Bias control access • Standard memory interface: <ul style="list-style-type: none"> • All I/O pins on one side • Power pins in metal 4 	<ul style="list-style-type: none"> • Column Redundancy • External timing tuning • Periphery power gating • Bit-wise write mask • Assist techniques • DFT (bypass, boundary scan) 	<ul style="list-style-type: none"> • Verilog • .lef • .lib (liberty, NLDM timing/power, CCS, AOCV, LVF) • EM/IR (Voltus PGV) • DFT (Tessent MBIST, ATPG) • UPF • CDL • GDSII

Compiler	High-Speed Low-Power SP	Ultra-High-Speed Low-Power SP
Key feature	30% – 50% lower power Area optimized	10% – 30% lower power Area optimized
Bitcell	HC	HC
Periphery VT	SLVT, LVT, RVT	SLVT, LVT, RVT
Operation range	0.5V-0.8V	0.8V-0.9V
Compiler Range	2kb – 1Mb	2kb – 1Mb
Words	64-32k	64-32k
Word size	16 - 144	16 - 144
Mux	4, 8	4, 8
Frequency range	1-2GHz	2.2-3.6GHz