# Xenergic's TSMC 22 Compiler

xenergic

| Compiler Features | Compiler Options | Supported BE/FE Models |
|---|---|---|
| • Single rail design<br>• Foundry bitcell based<br>• Four metal layers<br>• Standard memory interface:<br>  • All I/O pins on one side<br>  • Power pins in metal 4 | • Column Redundancy<br>• External timing tuning<br>• Periphery power gating<br>• Bit-wise write mask<br>• Assist techniques<br>• DFT (bypass, boundary scan) | • Verilog<br>• .lef<br>• .lib (liberty, NLDM timing/power, CCS, AOCV, LVF)<br>• EM/IR (Voltus PGV)<br>• DFT (Tessent MBIST, ATPG)<br>• UPF<br>• CDL<br>• GDSII |

| Compiler | Ultra-Low-Power SP | Low-Power SP | Low-Power TP |
|---|---|---|---|
| Key feature | 30% – 50% lower power<br>Area optimized | 30% – 50% lower power<br>Area optimized | 30% – 50% lower power<br>Area optimized |
| Process | ULP | LP | LP |
| Bitcell | ULLHD | HD | HD |
| Periphery VT | UHVT, SVT | SVT | SVT |
| Compiler Range | 2kb – 1Mb | 2kb – 1Mb | 2kb-64kb |
| Words | 64-32k | 64-32k | 64-2k |
| Word size | 16 - 144 | 16 - 144 | 16 - 144 |
| Mux | 4, 8 | 4, 8 | 4, 8 |
| Frequency range | 40-400MHz | 100-800MHz | 240-800MHz |

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