Xenergic's TSMC 40 Compiler

xenergic

Compiler Features	Compiler Options	Supported BE/FE Models

• Single rail design
• Foundry bitcell based
• Four metal layers
• Standard memory interface:
  • All I/O pins on one side
  • Power pins in metal 4
	• Column Redundancy
	• External timing tuning
	• Periphery power gating
	• Bit-wise write mask
	• Assist techniques
	• DFT (bypass, boundary scan)
		• Verilog
		• .lef
		• .lib (liberty, NLDM timing/power, CCS, AOCV, LVF)
		• EM/IR (Voltus PGV)
		• DFT (Tessent MBIST, ATPG)
		• UPF
		• CDL
		• GDSII

Compiler	Ultra-Low-Power SP	Low-Power SP
Key feature	30% – 50% lower power Area optimized	30% – 50% lower power Area optimized
Process	ULP	LP
Bitcell	ULLHD	HD
Periphery VT	EHVT, SVT	SVT
Compiler Range	2kb – 1Mb	2kb – 1Mb
Words	64-32k	64-32k
Word size	16 - 144	16 - 144
Mux	4, 8	4, 8
Frequency range	80-180MHz	250-600MHz

www.xenergic.com
Scheelevägen 15, 223 70 Lund, Sweden
+46 76-267 1820